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# Energy performance evaluation for dynamic frequency scaling on rate monotonic and earliest deadline first scheduling algorithm



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## ABSTRACT

Dynamic Voltage and Frequency Scaling (DVFS) algorithm is widely used to reduce processor's energy consumption in mixed-criticality systems. Existing works show that there are more DVFS algorithms were developed based on Earliest Deadline First (EDF) scheduling scheme compared to Rate Monotonic (RM) scheduling scheme. To understand the reason why EDF is prevalent for DVFS algorithms, simulation can be done to get the power consumption of both scheduling schemes. However, there is no simulation tools available dedicated for this purpose. This research aims to investigate power consumption of both scheduling schemes under different processor speed levels using SimSo simulator. The processor's utilization and schedulability are determined using a set of task in SimSo. Power consumption for Least Common Multiple of tasks period is then calculated based on the proposed power model. The result shows that EDF performs better than RM and able to reduce 30% of energy at processor speed of 0.7. In addition, the capability of SimSo to be used in DVFS algorithm creation also had been observed. It is found that SimSo can be used for further research with additional codes.

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## 1. Introduction

In the last decade, battery-powered embedded systems have become more important not only in the industries but also in our daily life. The advancement of microprocessor technology has improved processing performance and dramatically improves the size and capabilities of an embedded system. This has increased the energy requirement of such systems. In the applications such as wireless sensors network, wearable devices and mobile robots, it may be impossible to replace the battery to prolong the system's lifetime. The growth of battery density is also much slower than other technologies as shown in Fig. 1. Thus, the system's hardware and software need to be designed for energy efficiency.

There are two existing algorithms commonly used to reduce the energy consumption of embedded systems: Dynamic Voltage and Frequency Scaling (DVFS) and Dynamic Power Management (DPM). DVFS (Florence et al., 2016; Xu et al., 2012; Moreno and De Niz, 2012; Chen et al., 2013) reduces the processor energy usage by reducing processor

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frequency. This will slow down the processing speed and stretch the execution time as much as possible. Meanwhile, DPM (Deng et al, 2016; Awan and Petters, 2011; Huang et al., 2009) aims to reduce energy dissipation of the processor during idle time by shutting down the processors. This research is focusing on DVFS to understand how it can be applied efficiently.

From the literatures, it can be observed that most of DVFS algorithms are created based on EDF scheduler. This research tries to investigate the behavior of RM and EDF scheduling policies when the processor's speed is scaled to few different levels.

It is important to understand which scheduling policy is performed better for DVFS implementation in term of energy efficiency. The investigation is done using an open-source simulator, SimSo (Chéramy et al., 2014) to observe the schedulability of the task set. Then, energy consumption is determined based on the result. It is also important to see the feasibility of SimSo for DVFS research. This article is organized as follows: Section 2 discusses on the existing works related on the DVFS scheduling. The simulator, power model and task model are described in Section 3. Subsequent section will discuss on the result of the experiment. Finally, Section 5 concludes this article.

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Fig. 1: Growth of battery energy density compared to other technologies (Paradiso and Starner, 2005)

## 2. Related works

DVFS can be applied to static and dynamic priority scheduler. Rate Monotonic (RM) and Earliest Deadline First (EDF) scheduler (Liu and Layland, 1973) has been widely used for DVFS implementation. RM scheduling is a static priority scheduling scheme that gives highest priority to the task with the shortest period. Contrary, EDF is a dynamic priority scheduling that gives highest priority to the task with imminent deadline. EDF will keep sorting the tasks by its deadline and assigns the priority.

The first paper on DVFS, published in 1995, introduced three algorithms based on EDF scheduler (Yao et al., 1995). Those three algorithms were designed for aperiodic task. One of the algorithms that is known as Average Rate Heuristic, set the speed of processor equal to the sum of the worstcase utilization of the active jobs. It may affect the processing speed when there are few active tasks causing them finished after deadlines if additional task arrives. Pillai and Shin (2001) introduced five algorithms considering both EDF and RM schedulers. All the algorithms only consider periodic task and set the speed at the lowest speed that guaranteed execution time of the task.

Aydin is a researcher who presented five algorithms focusing on periodic tasks. Interestingly, all the algorithms are based on EDF scheduler. Aydin et al. (2001) proposed an  $O(n^2 \log n)$  algorithm to compute optimal speed values for task execution. It proves that every task can execute at constant speed without affecting the energy optimality. Aydin et al. (2004) proposed another three algorithms which are offline algorithm, online algorithm that dynamically reclaim energy and an algorithm that is using online, adaptive and speculative speed adjustment mechanism. The researcher continues his work (Aydin et al., 2006) by proposing an algorithm with more general power model that includes leakage power, frequency-dependent power and frequencyindependent power components. In recent years, Bambagini et al. (2011) introduced enhanced algorithms, BSDVFS and BSDVFS\* which are based on EDF scheduler. The algorithms consider switching speed overhead by checking the period of dynamic slack.

## 3. Methodology

This section explains the power model used in the experiment to determine processor's power consumption. Then, the workload model is presented. At the end of the section, the SimSo simulator and the experiment are described.

## 3.1. Power model

This experiment considers a periodic real-time task set running on a single processor system. The processor is assumed to have DVFS mechanisms allowing it to dynamically adjust its operating frequency. It has several speed levels that represents the total number of frequencies supported by the processor. Consider a real-time task with execution time, t running on a processor at maximum frequency,  $f_{max}$ . The processor can be scaled to run at a several frequency levels, f where  $0 < f \le f_{max}$ . So, the relative processor speed level s can be defined as  $f/f_{max}$ .

Processor's power consumption is composed of static and dynamic power. Static power consumption is the power dissipated during by processor during no activities. While, dynamic power consumption is the power consumed during task executions. This experiment only considers the dynamic power consumption which can be managed by the DVFS mechanism. Most of early DVFS algorithms assumed dynamic power is generally in proportion to the cubic of the speed, s. Therefore, energy consumption, E for a given execution time, t is defined by

$$E = \alpha \cdot \frac{t}{s} \cdot s^3 \tag{1}$$

$$E = \alpha \cdot t \cdot s^2 \tag{2}$$

where  $\alpha$  is a coefficient (Ali et al., 2015). For this experiment,  $\alpha$  is assumed equals to 1 for the sake of simplicity.

#### 3.2. Task model

The task model for the experiment consists of independent tasks which are characterized by a 3tuple of parameters: a period P, a deadline D, and a Worst-Case Execution Time (WCET) C. Tasks are released simultaneously after processor start execution. The task set used in the experiment (Bambagini et al., 2016) is shown in Table 1.

The utilization of the tasks,  $U_i$  can be calculated using the following formula (Buttazzo, 2005):

$$U_i = C/P \tag{3}$$

and processor's utilization, UP is defined as

$$U_P = \sum_{i=1}^n U_i \tag{4}$$

where  $U_P$  is equal to 0.7.

## 3.3. Simulation

The experiment was done using a simulator called SimSo (Simulation of Multiprocessor Scheduling with Overheads) which is developed by the researchers in Laboratory for Analysis and Architecture of System, (LAAR) in France. SimSo is an open-source simulator developed using Python programming language. It means that researchers are able to extend its functionality based on their preferences.

The task set in Table 1 is inserted into the SimSo. All tasks are set to be aborted if they missed their deadlines. Fig. 2 shows the tasks that have been keyed in. Simulation is then set to run in five processor speed level: 0.6, 0.7, 0.8, 0.9 and 1.0. Speed level below 0.5 is not tested because it is not energy efficient (Bambagini et al., 2016) and increases the risk of missing deadline.

Qt N	/odel data									
Gene	eral Sch	eduler	Proce	ssors	Tasks					
id	Name	Task ty	ype	Abort	on miss	Act. Date (ms)	Period (ms)	ct. da	Deadline (ms)	WCET (ms)
1	TASK T1	Periodic	•	🗹 Yes		0.0	50.0	-	50.0	20.0
2	TASK T2	Periodic	•	🗹 Yes		0.0	100.0	-	100.0	20.0
3	TASK T3	Periodic	•	🗹 Yes		0.0	150.0	-	150.0	15.0
<										>
						Edit data fields				
Ħ,	Remove sele	cted task(	s)						Add task Gen	erate Task Set



Simulation is done using RM and EDF scheduling for each speed level. Duration of simulation is the Least Common Multiple of periods that is 300ms. Processor's utilization is determined and energy consumption for every case is calculated. Finally, the functionality and capability of SimSo for DVFS algorithm have been analyzed.

	Table 1	<b>l:</b> Task set	
Task	Period, P	Deadline, D	WCET, C
T1	50	50	20
T2	100	100	20
Т3	150	150	15

#### 4. Results and analysis

The results are divided into three components. First, result on simulation of RM and EDF at maximum processor speed. Second, result on simulation at different speed level. Finally, a comparison with the result of DVFS algorithm is shown.

## 4.1. RM and EDF at maximum speed

Simulation shows that both scheduling scheme successfully shows the processor's utilization similar as calculated. Fig. 3 shows the simulation result of RM and EDF which is exactly similar.



Fig. 3: Simulation result of RM and EDF at maximum speed

## 4.2. RM and EDF at different speed level

Simulation shows that both scheduling scheme perform similarly at speed 0.8 and 0.9. However, RM fails to schedule at speed lower than that. EDF still able to schedule at speed 0.7 at maximum processor's utilization and energy consumption is reduced by 30%. Table 2 summarizes the result of simulation. Fig. 4 and Fig. 5 show the results for both scheduling schemes at speed 0.7 respectively.

## 4.3. DVFS algorithm using SimSo

SimSo provides two built-in DVFS algorithms: Static EDF and Cycle Conserving EDF (CC-EDF). Simulation for both algorithms depicts the similar result as shown as Fig. 5. Task allocation of the algorithms is shown in Fig. 6. However, there is no information on processor speed in the simulation result. Researcher only knows whether the task set is schedulable or not. To have this information, SimSo needs to be amended using the Python codes.



Fig. 4: RM fails to schedule Task 3 at speed 0.7

## 5. Conclusion and future work

This paper investigates the processor's utilization of RM and EDF algorithms using SimSo simulator. Based on the task set, it is observed that EDF performs better than RM at a lower speed. At the minimum schedulable speed, energy consumption of EDF is reduced by 30% compared to RM which is only reduced 20%. Result also shows the advantage of EDF that allows full processor utilization, which implies a more efficient exploitation of computational resources. SimSo also able to schedule based on DVFS algorithm but amendment needs to be done to the codes so that more information can be displayed to users. As a conclusion, SimSo can be used as simulator for a research on designing a DVFS algorithm with additional coding.

Table	2: Simulation	result for	different s	need level
rabic	<b>L</b> . Simulation	i coult loi	unici chit s	

Drogogoan Croad	Rate Mono	otonic Schedu	ling	Earliest Deadline First						
Processor speed	Energy Consumption	Utilization	Schedulability	Energy Consumption	Utilization	Schedulability				
0.6	107.9998	1.000	No	107.9998	1.000	No				
0.7	125.9999	0.8571	No	146.9998	1.000	Yes				
0.8	168	0.8750	Yes	168	0.8750	Yes				
0.9	188.9998	0.7778	Yes	188.9998	0.7778	Yes				
1.0	210	0.700	Yes	210	0.7	Yes				

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Ó	10	20	30	40	50	60	70	80	90	1Ó0	110	120	130	140	150	160	170	180	190	200	210	220	230	240	250	260	270	280	290	300
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' <b>∠</b> 1					1					1					1					1					1					- 1
AS					1					1															1					- 1
EF-	10	20	20	40		60	70			100	110	120	120	140	150	160	170	100	100	200	210	220	220	240	250	260	270	200	200	
~	10	20	50	40	- 00	00	/0	00	90	100	110	120	100	140	100	100	1/0	100	190	200	210	220	200	240	200	200	2/0	200	290	500
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ЖI																														- 1
ZL.																							_							
' ó '	10	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160	170	180	190	200	210	220	230	240	250	260	270	280	290	300
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**Fig. 5:** EDF utilize 100% of processor at speed 0.7

Results						0 Result	s						
General	Logs	Tasks	Sche	eduler	Processors	General	Logs	Tasks	Scheduler	Processors			
General	TASK T	1 TA	SK T2	TASK T	3	Schedu	uling even	ts:					
Computatio	on time:					schedu	le count:	25					
Task TASK T1	min 28.571	avg 28.571	max 28.571	std dev 0.000	occupancy 0.571	on_act	on_activate count: 14 on_terminate count: 11						
TASK T2	28.571	28.571	28.571	0.000	0.286	Schedu	uling overl	head:					
TASK T3	21.429	21.429	21.429	0.000	0.143	schedu on_act on_ter Sum:	ule overhe tivate over minate ov 0.0000ms	ead: 0.0000 rhead: 0.00 verhead: 0. (0 cycles)	0ms (0 cycles) 000ms (0 cycle: 0000ms (0 cyc	s) les)			
Preemption	ns:					- Timers							
Migrations:	1					CPU I							
Task migra	tions:												
Response t	ime:												

Fig. 6: Task allocation of Static-EDF and CC-EDF

In the future, the author will work on an EDFbased DVFS algorithm to reduce energy consumption of mixed-criticality systems. SimSo may provide a good foundation for author as a task simulator. It can help author to save time from creating new simulator from scratch. However, the real hardware implementation is important to prove the proposed algorithms.

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